```
MMM         MMM     CCCCCCCCCCCC  LLL              DDDDDDDDDDDD     RRRRRRRRRRRR
MMM         MMM     CCCCCCCCCCCC  LLL              DDDDDDDDDDDD     RRRRRRRRRRRR
MMM         MMM     CCCCCCCCCCCC  LLL              DDDDDDDDDDDD     RRRRRRRRRRRR
MMMMMM   MMMMMM  CCC              LLL              DDD         DDD  RRR         RRR
MMMMMM   MMMMMM  CCC              LLL              DDD         DDD  RRR         RRR
MMMMMM   MMMMMM  CCC              LLL              DDD         DDD  RRR         RRR
MMM   MMM   MMM  CCC              LLL              DDD         DDD  RRR         RRR
MMM   MMM   MMM  CCC              LLL              DDD         DDD  RRR         RRR
MMM   MMM   MMM  CCC              LLL              DDD         DDD  RRR         RRR
MMM         MMM  CCC              LLL              DDD         DDD  RRRRRRRRRRRR
MMM         MMM  CCC              LLL              DDD         DDD  RRRRRRRRRRRR
MMM         MMM  CCC              LLL              DDD         DDD  RRRRRRRRRRRR
MMM         MMM  CCC              LLL              DDD         DDD  RRR   RRR
MMM         MMM  CCC              LLL              DDD         DDD  RRR   RRR
MMM         MMM  CCC              LLL              DDD         DDD  RRR   RRR
MMM         MMM  CCC              LLL              DDD         DDD  RRR      RRR
MMM         MMM  CCC              LLL              DDD         DDD  RRR      RRR
MMM         MMM  CCC              LLL              DDD         DDD  RRR      RRR
MMM         MMM     CCCCCCCCCCCC  LLLLLLLLLLLLLLL  DDDDDDDDDDDD     RRR         RRR
MMM         MMM     CCCCCCCCCCCC  LLLLLLLLLLLLLLL  DDDDDDDDDDDD     RRR         RRR
MMM         MMM     CCCCCCCCCCCC  LLLLLLLLLLLLLLL  DDDDDDDDDDDD     RRR         RRR
```

```
LL            AAAAAA    DDDDDDDD    MM      MM  DDDDDDDD    TTTTTTTTTT
LL            AAAAAA    DDDDDDDD    MM      MM  DDDDDDDD    TTTTTTTTTT
LL          AA      AA  DD      DD  MMMM  MMMM  DD      DD      TT
LL          AA      AA  DD      DD  MMMM  MMMM  DD      DD      TT
LL          AA      AA  DD      DD  MM  MM  MM  DD      DD      TT
LL          AA      AA  DD      DD  MM  MM  MM  DD      DD      TT
LL          AA      AA  DD      DD  MM      MM  DD      DD      TT
LL          AAAAAAAAAA  DD      DD  MM      MM  DD      DD      TT
LL          AAAAAAAAAA  DD      DD  MM      MM  DD      DD      TT
LL          AA      AA  DD      DD  MM      MM  DD      DD      TT          ....
LL          AA      AA  DD      DD  MM      MM  DD      DD      TT          ....
LLLLLLLLLL  AA      AA  DDDDDDDD    MM      MM  DDDDDDDD      TT          ....
LLLLLLLLLL  AA      AA  DDDDDDDD    MM      MM  DDDDDDDD      TT          ....

LL            IIIIII      SSSSSSSS
LL            IIIIII    SSSSSSSS
LL              II      SS
LL              II      SS
LL              II      SS
LL              II      SS
LL              II        SSSSSS
LL              II        SSSSSS
LL              II              SS
LL              II              SS
LL              II              SS
LL              II              SS
LLLLLLLLLL    IIIIII    SSSSSSSS
LLLLLLLLLL    IIIIII    SSSSSSSS
```

```
                        .TITLE  LADMDT - LPA-11 DEDICATED MODE DISPATCH TABLE
                        .IDENT  'V04-000'
                ;
                ;
                ;*****************************************************************************
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                ;*                                                                           *
                ;*****************************************************************************
                ;
                ;
                ; CHARLES A. SAMUELSON
                ; FEBRUARY 4, 1977
                ;
                ; MODIFIED BY:
                ;       V02-004 SRB0003         Steve Beckhardt         3-Sep-1980
                ;               Changed value of SEX parameter from ^0120 to ^020.
                ;
                ;+
                ; DMDT -- DEDICATED MODE DISPATCH TABLE
                ; TABLE FOR LPA11 MICRO PROCESSOR DEDICATED MODE SAMPLING
                ;-
                ;
00000000        .PSECT  _LPA$CODE,NOWRT,WORD

                ; DEFINED VALUES
                ;
00000012        DMDSIZ=18.              ;LENGTH OF DMDT BUFFER IN BYTES
00000040        SDT=^O100               ;SLAVE DISPATCH TABLE START ADDRESS
00000000        CAINC=0                 ;CHANNEL ADDRESS INCREMENT VALUE
00000000        AD1SRL=0                ;ADC #1 STATUS REGISTER ADDRESS LOW BYTE
00000010        SEX=^O20                ;SELECT EXTERNAL CLOCK START
0000001D        RONPR=^O35              ;REQUEST OUTPUT NPR IN MICRO-PROCESSOR
00000000        CLR=0                   ;CLEAR AD STATUS REGISTER
0000009D        RONPRL=^O235            ;REQUEST OUTPUT NPR LOW BYTE IN MICRO-PROCESSOR
00000002        AD1DRL=2                ;ADC #1 DATA REGISTER ADDRESS LOW BYTE
0000000D        RINPR=^O15              ;REQUEST INPUT NPR
00000020        SCS=^O40                ;SELECT CLOCK OVERFLOW START FOR ADC'S
00000020        AD2SRL=^O40             ;ADC #2 STATUS REGISTER ADDRESS LOW BYTE
00000022        AD2DRL=^O42             ;ADC #2 DATA REGISTER ADDRESS LOW BYTE
```

```
                     00000001  0000    58 AD1SRH=1                    ;ADC #1 STATUS REGSITER HIGH BYTE ADDRESS
                     00000021  0000    59 AD2SRH=^O41                 ;ADC #2 STATUS REGISTER HIGH BYTE ADDRESS
                     00000010  0000    60 SEN=^O20                    ;SELECT EXTERNAL START, NO INTERRUPT ENABLE
                               0000    61 ;
                               0000    62 ;
                               0000    63 LPA$$DMDT::
                               0000    64 D.OES::                     ;ONE ADC, EXTERNAL TRIGGER, SINGLE CHANNEL
   40 9D 00 0D 02 1D 10 00 72  0000    65          .BYTE   DMDSIZ+<3*^O40>,AD1SRL,SEX,RONPR,AD1DRL,RINPR,CLR,RONPRL,SDT
                     00000013  0009    66 .=D.OES+^O23
                               0013    67 D.OEQ::                     ;ONE ADC, EXTERNAL TRIGGER, SEQUENTIAL CHANNEL
40 9D 00 0D 02 1D 10 00 00 72  0013    68          .BYTE   DMDSIZ+<3*^O40>,CAINC,AD1SRL,SEX,RONPR,AD1DRL,RINPR,CLR,RONPRL,SDT
                           00  001D    69          .BYTE   CAINC
                     00000026  001E    70 .=D.OEQ+^O23
                               0026    71 D.OCS::                     ;ONE ADC, CLOCK TRIGGER, SINGLE CHANNEL
   40 9D 00 0D 02 1D 20 00 72  0026    72          .BYTE   DMDSIZ+<3*^O40>,AD1SRL,SCS,RONPR,AD1DRL,RINPR,CLR,RONPRL,SDT
                     00000039  002F    73 .=D.OCS+^O23
                               0039    74 D.OCQ::                     ;ONE ADC, CLOCK TRIGGER, SEQUENTIAL CHANNEL
40 9D 00 0D 02 1D 20 00 00 72  0039    75          .BYTE   DMDSIZ+<3*^O40>,CAINC,AD1SRL,SCS,RONPR,AD1DRL,RINPR,CLR,RONPRL,SDT
                           00  0043    76          .BYTE   CAINC
                     0000004C  0044    77 .=D.OCQ+^O23
                               004C    78 D.TES::                     ;TWO ADC, EXTERNAL TRIGGER, SINGLE CHANNEL
   48 9D 00 0D 02 1D 10 00 72  004C    79          .BYTE   DMDSIZ+<3*^O40>,AD1SRL,SEX,RONPR,AD1DRL,RINPR,CLR,RONPRL,SDT+^O10
      40 9D 00 0D 22 1D 10 20  0055    80          .BYTE   AD2SRL,SEX,RONPR,AD2DRL,RINPR,CLR,RONPRL,SDT
                     0000005F  005D    81 .=D.TES+^O23
                               005F    82 D.TEQ::                     ;TWO ADC, EXTERNAL TRIGGER, SEQUENTIAL CHANNEL
      9D 00 0D 02 1D 10 00 00 72  005F 83          .BYTE   DMDSIZ+<3*^O40>,CAINC,AD1SRL,SEX,RONPR,AD1DRL,RINPR,CLR,RONPRL
   40 9D 00 0D 22 1D 10 20 00 49  0068 84          .BYTE   SDT+^O11,CAINC,AD2SRL,SEX,RONPR,AD2DRL,RINPR,CLR,RONPRL,SDT
                     00000072  0072    85 .=D.TEQ+^O23
                               0072    86 D.TCS::                     ;TWO ADC, CLOCK TRIGGER, SINGLE CHANNEL
      9D 00 0D 02 1D 20 00 B2  0072    87          .BYTE   DMDSIZ+<5*^O40>,AD1SRL,SCS,RONPR,AD1DRL,RINPR,CLR,RONPRL
   40 9D 00 0D 22 1D 20 20 48  007A    88          .BYTE   SDT+^O10,AD2SRL,SCS,RONPR,AD2DRL,RINPR,CLR,RONPRL,SDT
                     00000085  0083    89 .=D.TCS+^O23
                               0085    90 D.TCQ::                     ;TWO ADC, CLOCK TRIGGER, SEQUENTIAL CHANNEL
      9D 00 0D 02 1D 20 00 00 B2  0085 91          .BYTE   DMDSIZ+<5*^O40>,CAINC,AD1SRL,SCS,RONPR,AD1DRL,RINPR,CLR,RONPRL
40 9D 00 0D 22 1D 20 20 00 49  008E    92          .BYTE   SDT+^O11,CAINC,AD2SRL,SCS,RONPR,AD2DRL,RINPR,CLR,RONPRL,SDT
                     00000098  0098    93 .=D.TCQ+^O23
                               0098    94 ;
                               0098    95 ; PARALLEL MODE TABLE
                               0098    96 ;
                               0098    97 D.TESP::                    ;TWO ADC, EXTERNAL TRIGGER, SINGLE, PARALLES
   0D 02 1D 10 20 1D 00 10 12  0098    98          .BYTE   DMDSIZ+<0*^O40>,SEX,AD1SRL,RONPR,AD2SRL,SEN,RONPR,AD1DRL,RINPR
      46 9D 21 9D 01 0D 22     00A1    99          .BYTE   AD2DRL,RINPR,AD1SRH,RONPRL,AD2SRH,RONPRL,SDT+6
                     000000AB  00A8   100 .=D.TESP+^O23
                               00AB   101 D.TEQP::                    ;TWO ADC, EXTERNAL TRIGGER, SEQUENTIAL, PARALLEL
   02 00 1D 10 20 1D 00 10 12  00AB   102          .BYTE   DMDSIZ+<0*^O40>,SEX,AD1SRL,RONPR,AD2SRL,SEN,RONPR,CAINC,AD1DRL
      46 9D 21 9D 01 0D 22 0D  00B4   103          .BYTE   RINPR,AD2DRL,RINPR,AD1SRH,RONPRL,AD2SRH,RONPRL,SDT+6
                     000000BE  00BC   104 .=D.TEQP+^O23
                               00BE   105 D.TCSP::                    ;TWO ADC, CLOCK TRIGGER, SINGLE, PARALLEL
   0D 02 1D 20 20 1D 00 20 92  00BE   106          .BYTE   DMDSIZ+<4*^O40>,SCS,AD1SRL,RONPR,AD2SRL,SCS,RONPR,AD1DRL,RINPR
      46 9D 21 9D 01 0D 22     00C7   107          .BYTE   AD2DRL,RINPR,AD1SRH,RONPRL,AD2SRH,RONPRL,SDT+6
                     000000D1  00CE   108 .=D.TCSP+^O23
                               00D1   109 D.TCQP::                    ;TWO ADC, CLOCK TRIGGER, SEQUENTIAL, PARALLEL
   02 00 1D 20 20 1D 00 20 92  00D1   110          .BYTE   DMDSIZ+<4*^O40>,SCS,AD1SRL,RONPR,AD2SRL,SCS,RONPR,CAINC,AD1DRL
      46 9D 21 9D 01 0D 22 0D  00DA   111          .BYTE   RINPR,AD2DRL,RINPR,AD1SRH,RONPRL,AD2SRH,RONPRL,SDT+6
                               00E2   112
                     00000100  00E2   113          .BLKB   30                      ; PAD OUT TO 256 BYTES
                               0100   114
```

```
0100   115          .END
```

```
AD1DRL          = 00000002
AD1SRH          = 00000001
AD1SRL          = 00000000
AD2DRL          = 00000022
AD2SRH          = 00000021
AD2SRL          = 00000020
CAINC           = 00000000
CLR             = 00000000
D.OCQ             00000039 RG    01
D.OCS             00000026 RG    01
D.OEQ             00000013 RG    01
D.OES             00000000 RG    01
D.TCQ             00000085 RG    01
D.TCQP            000000D1 RG    01
D.TCS             00000072 RG    01
D.TCSP            000000BE RG    01
D.TEQ             0000005F RG    01
D.TEQP            000000AB RG    01
D.TES             0000004C RG    01
D.TESP            00000098 RG    01
DMDSIZ          = 00000012
LPA$$DMDT         00000000 RG    01
RINPR           = 0000000D
RONPR           = 0000001D
RONPRL          = 0000009D
SCS             = 00000020
SDT             = 00000040
SEN             = 00000010
SEX             = 00000010
```

Psect synopsis

PSECT name	Allocation	PSECT No.	Attributes
. ABS .	00000000 (0.)	00 (0.)	NOPIC USR CON ABS LCL NOSHR NOEXE NORD NOWRT NOVEC BYTE
_LPA$CODE	00000100 (256.)	01 (1.)	NOPIC USR CON REL LCL NOSHR EXE RD NOWRT NOVEC WORD

Performance indicators

Phase	Page faults	CPU Time	Elapsed Time
Initialization	29	00:00:00.07	00:00:00.26
Command processing	100	00:00:00.43	00:00:01.44
Pass 1	67	00:00:00.60	00:00:01.25
Symbol table sort	0	00:00:00.01	00:00:00.01
Pass 2	38	00:00:00.28	00:00:01.45
Symbol table output	4	00:00:00.04	00:00:00.04
Psect synopsis output	1	00:00:00.02	00:00:00.02
Cross-reference output	0	00:00:00.00	00:00:00.00
Assembler run totals	242	00:00:01.46	00:00:04.48

The working set limit was 900 pages.
2394 bytes (5 pages) of virtual memory were used to buffer the intermediate code.

There were 10 pages of symbol table space allocated to hold 29 non-local and 0 local symbols.
115 source lines were read in Pass 1, producing 11 object records in Pass 2.
6 pages of virtual memory were used to define 0 macros.

+-----------------------------+
! Macro library statistics !
+-----------------------------+

Macro library name	Macros defined
_255DUA28:[SYSLIB]STARLET.MLB;2	0

0 GETS were required to define 0 macros.

There were no errors, warnings or information messages.

```
MACRO/LIS=LIS$:LADMDT/OBJ=OBJ$:LADMDT MSRC$:LADMDT/UPDATE=(ENH$:LADMDT)
```

MCLDR

MDL32

LALOAD
MAP

MDL32
MAP

XFLOADER
MAP

LALOADER
LIS

XFLOADER
LIS

LADAMCODE
LIS

LALOAD
LIS

MARBLI

MARBLI
MAP

LALOADER
MAP

LAMRMCODE
LIS

LAADMCODE
LIS

MARBLI
LIS

LADMDT
LIS